الجامعة الافتراضية السورية
SYRIAN VIRTUAL UNIVERSITY

Course definition

Computer Architecture 2

Information

Technology

Engineering

Powered by: KNOWLGICA KNOWLEDGE SOLUTIONS & TECH

1. Basic Information:

Course Name	Computer Architecture 2
Course ID	NCA601
No. of Recorded Sessions*	12
No. of Synchronized Sessions*	18
No. of Quizzes (hrs.)	
Exam (hrs.)	
Registered Sessions Work Load (hrs.)	36
Synchronized Sessions Work Load (hrs.)	48
Credit Hours	6

* The duration of each session 1.5 hr

2. Pre-Requisites:

Course	ID
Computer Architecture 1	BCA 501

3. Course Objectives:

This course aims to introduce the student to the language of the assembly that is used within processors, and to link with what has been learned within the computer architecture (1) regarding the structure of the distribution of memories within the computer system, and how to achieve functional connectivity within computer systems. It also aims to familiarize the student with how to achieve processing and how to raise the performance of computer systems by employing what has been learned within this course and the computer architecture (1) course.

In particular, the student will be able to:

1. Examine how to achieve shared memory when working within a multiprocessing environment.
2. The ability to handle errors and achieve reliability.
3. Achieving instruction level parallelism.
4. Knowing how the cache holds together in multiprocessing.
5. The scalability of the computer system architecture.

4. Learning Outcomes (LO):

By the end of this course the learner is expected to:

- Have an overview of the basic characteristics of machine instructions.
- Describe the different types of addressing patterns that are common in instruction sets.
- Distinguish between user visual records and control/status records, and target records within each category.
- Have an overview of research findings on the instruction execution characteristics that motivated the development of the RISC approach.
- Explain the difference between ultrafast and super-fast approaches.
- Distinguishing the types of parallel processor organizations.
- Understand the hardware performance issues that prompted the move to multi-core computers.
- Provide an overview of CUDA.

5. Assessment Results:

Chapter No.	Chapter Title	Intended Objectives	Assessment Type				
			Developed content/ Recorded Sessions	Practical Activities (Synchronized Sessions)	Quizzes and Exams	Presentations And Interviews	Reports
CH1	Instruction sets	Comprehension –Analytical Thinking	X	X	X		
CH2	Computer language	Comprehension –Analytical Thinking – Tools And Application Hands– On	X	X	X		X
CH3	Performance enhancement using Parallelism	Comprehension –Analytical Thinking – Tools And Application Hands– On	X	X	X		X
CH4	Parallel	Comprehensi	X	X	X		X

	processing and multi–core computing	on –Analytical Thinking – Tools And Application Hands– On					
CH5	Control unit	Comprehensi on –Analytical Thinking – Tools And Application Hands– On	X	X	X		X

6. Course Syllabus

Chapter No.	Chapter Title	Chapter Content (Syllabus)	No. of Theoretical Learning Units	No. of Practical Learning Units)
CH1	Instruction sets	• Instruction set characteristics • ARM data types • ARM operation types • ARM addressing types • ARM instruction formats	1	1
CH2	Computer language	1 . Hardware processes 2 . MIPS addressing 3 . Compiler optimization 4 . Object oriented languages	2	2
CH3	Performance enhancement using Parallelism	• Pipelining • Data Hazards • Branching hazards • Hardware description language • Exceptions • Parallelism • Superscala • VLIW	4	4
CH4	Parallel processing and multi–	1.Multiprocessing organization 2.symmetrical multi–processing 3.clusters	3	3

	core computing	4.Unregularly memory access 5.cloud computing 6.ARM Cortex-A15 7.IBM EC12 8.Multi-purpose data handling units		
CH5	Control unit	1.Micro-operation 2.Hardware implementation 3.microinstruction sequencing 4.TI 8800	3	3

7. Practical Activity:

- Tools and Labs:

Tool Name	Description
Word, excel, internet browsers	Available

- Practical Activities per Chapters:

Chapter	Practical Activity	Remarks
CH1	☒ Exercises ☒ Homework ☐ Webinars ☐ Project ☐ Experiment ☐ Other	Homework
CH2	☒ Exercises ☒ Homework ☐ Webinars ☐ Project ☐ Experiment ☐ Other	Homework
CH3	☒ Exercises ☒ Homework Webinars	Homework

	☐ Project ☐ Experiment ☐ Other	
CH4	☒ Exercises ☒ Homework ☐ Webinars ☐ Project ☐ Experiment ☐ Other	Homework
CH5	☒ Exercises ☒ Homework ☐ Webinars ☐ Project ☐ Experiment ☐ Other	Homework

5.References:

1. "Computer Organization and Architecture *Designing for Performance* Tenth Edition", William Stallings, Pearson Education, Hoboken 2016.
2. "Computer Organization and Design THE HARDWARE/SOFTWARE INTERFACE", David A. Patterson, John L. Hennessy. Elsevier Inc, USA 2014.