الجامعة الافتراضية السورية
SYRIAN VIRTUAL UNIVERSITY

Computer Architecture 1

Course definition

Information

Technology

Engineering

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1. Basic Information:

Course Name	Computer Architecture 1
Course Code	BCA501
Number of Presentational Sessions*	10×2
Number of Synchronous Sessions**	10
Number of Shorter Tests***	3
Number of Exams***	1
Theoretical Sessions Work Load (hrs.)	36
Practical Sessions Work Load (hrs.)	48
Credit Hours	6

***Each presentational session comprises both recorded lecture (1.5 hrs.) and interactive learning content (1.5 hrs).**

****Each synchronous session comprises the interactive lecture carried out in real time in a virtual class (1.5 hrs).**

*****Each shorter test is 0.5 hr. long. The final exam is 2 hrs. long.**

N.B.

Generally, each chapter requires two presentational sessions: one for the recorded content and one for the interactive content (unless the chapter is too long, in which case it may require more sessions). This note applies to synchronous sessions as well, where each chapter requires one synchronous session generally.

2. Prerequisites courses:

Course	ID
Logical circuits	BLC401

3. Course Objectives:

Computer Architecture 1 aim to acquaint the student with evolution of processor design of modern processors, its performance calculation, instruction set design and execution. In addition, the student will know the memory types in modern computers and how it is related to the computer performance.

In particular the student will be able to:

1. Study of top down computer structure and functions
2. Understand the performance of processor
3. Develop assembly programs and understand its execution
4. Study the mapping technics of cache/main memories
5. Be familiar with arithmetic operations in processors

4. Learning Outcomes:

By the end of this course the learner is expected to:

1. Study of the historical evolution of processor design and the most important modern technics.
2. Study of computer performance.
3. Top down study of computer structure and functions (central processing unit, main memory, I/O, system bus).
4. Study the instruction cycle and the execution steps of an assembly program.
5. Deep study of main/cache design, description, mapping methods, write policy, and performance of modern caches.
6. Study of main memory types and performance.
7. Study of number system in computers
8. Study of arithmetic operations in processors.

5. Assessment Results:

Chapter Number	Chapter Title	General Objectives	Assessment Type				
			Interactive Content & Recorded Sessions	Applied Activities (Synch. Sessions)	Final Exam*/ Shorter Tests**	Presentations And Interviews ***	Reports ***
CH1	Basic concepts in the evolution of computer technology and performance	Comprehension –Analytical Thinking	✓	✓	✓	✓	✓
CH2	Hierarchical view of computer structure and functions	Comprehension –Analytical Thinking –Tools And Application Hands– On	✓	✓	✓	✓	✓
CH3	Cache memory	Comprehension –Analytical Thinking –Tools And Application Hands– On	✓	✓	✓	✓	✓
CH4	Main memory	Comprehension –Analytical	✓	✓	✓	✓	✓

		Thinking –Tools And Application Hands– On					
CH5	Computer arithmetic operations	Comprehension –Analytical Thinking –Tools And Application Hands– On	✓	✓	✓	✓	✓

***The final exam is two hours long and is given at the end of the course.**

****Shorter tests are about 30 minutes long and are given after three or four lectures throughout the semester during synchronous sessions.**

*****Presentations, interviews, and reports are submitted once after each three or four lectures throughout the semester during synchronous sessions.**

6. Course Syllabus

Chapter	Subject	Content	Number of Learning Objects	Number of synchronous Learning Objects
CH1	Basic concepts in the evolution of computer technology and performance	1. The computer architecture of modern computers 2. Computer structure and functions 3. The evolution of computer technology from vacuum tubes to cloud computing 4. The evolution of microcontrollers 5. Performance measures • Clock Speed • Instruction execution rate • MIPS rate	5	2
CH2	Hierarchical view of computer structure and functions	1. Computer component 2. Computer function 3. Interconnection structures 4. Bus interconnection 5. Point-point interconnection 6. PCI express	6	3
CH3	Cache memory	1. Computer memory system Overview 2. Cache memory principals • Single/multi-level cache • Cache/main memory structure • Cache read operation	3	2

		3. Elements of cache design • Size • Addresses • Mapping function ▪ Direct ▪ Associative ▪ Set associative • Write policy • Line size • Number of caches		
CH4	Main memory	1. Description of semiconductor memories 2. What is SRAM, and DRAM? 3. Description and types of read only memory 4. Description of read mostly memories, EPROM, EEPROM, Flash 5. Error correction codes 6. Structure of modern dynamic RAM (DDR DRAM) 7. Flash memory	7	3
CH5	Computer arithmetic operations	1. Binary system 2. Hexadecimal system 3. Converting between binary and decimal system	8	4

		4. The arithmetic and logic unit 5. Integer representation 6. Integer arithmetic 7. Floating point representation 8. Floating point arithmetic		

7. Practical Activity:

- **Tools and Labs:**

Tool Name	Description
Word, excel, internet browsers	Available

- **Practical Activities per Chapters:**

Chapter	Activities Type	Remarks
CH1	☑ Exercises ☑ Homework ☐ Webinars ☐ Project ☑ Experiment ☐ Other	Homework
CH2	☑ Exercises ☑ Homework ☐ Webinars ☐ Project ☑ Experiment ☐ Other	Homework
CH3	☑ Exercises ☑ Homework ☐ Webinars ☐ Project ☑ Experiment ☐ Other	Homework
CH4	☑ Exercises	

	☑ Homework ☑ Webinars ☐ Project ☑ Experiment ☐ Other	Homework
CH5	☑ Exercises ☑ Homework ☐ Webinars ☐ Project ☑ Experiment ☐ Other	Homework

8. References:

1. Computer Organization and Arch
2. itecture Designing for Performance Tenth Edition", William Stallings, Pearson Education, Hoboken 2016.
3. Computer Organization and Design THE HARDWARE/SOFTWARE INTERFACE", David A. Patterson, John L. Hennessy. Elsevier Inc, USA 2014.